Amendments to the Specification:

Please replace the paragraph beginning at page 1, line 2 with the following amended paragraph:

This application is a continuation of U.S. application serial no. 09/473,113, filed on December 28, 1999 (now U.S. Patent No. 6,631,430); the disclosure of which is considered part of (and is incorporated by reference in) the disclosure of this application.

Please replace the existing title "OPTIMIZATIONS TO RECEIVE PACKET STATUS FROM FIFO BUS" beginning at page 1, line 1 with the following amended title:

BUS INTERFACE WITH A FIRST-IN-FIRST-OUT MEMORY

Please delete previous abstract at page 14 and add the following new abstract:

A system includes a multithreaded processor. The multithreaded processor includes a plurality of microengines, a memory controller, a first bus interface and a second bus interface. The second bus interface includes a first-in-first-out memory with a plurality of elements to store packet data and packet status. The system also includes a system bus coupled to the first bus interface and a network bus coupled to the second bus interface.